Remarks

The Office Action dated 18 June 2002 has been received and reviewed. Claims 27, 32, and 36 were amended. The pending claims are claims 27-44. Reconsideration and withdrawal of the rejections are respectfully requested.

Claim Amendments

Claims 27 and 32 were amended to recite a chemical vapor codeposited diffusion barrier layer. Support for this amendment may be found in the Specification of the present invention, e.g., at page 9, line 23 through page 11, line 24.

Claim 36 was amended to correct a typographical error.

The 35 U.S.C. § 102 Rejections

The Examiner rejected claims 27-35 under 35 U.S.C. § 102(b) as being anticipated by Matsubara et al. (U.S. Patent No. 5,122,923).

Applicants traverse this rejection and submit that claims 27-35 are not anticipated by Matsubara et al. because such document does not teach each and every element of claims 27-35. For a claim to be anticipated under 35 U.S.C. § 102(b), each and every element of the claim must be found in a single prior art reference. *See* M.P.E.P. § 2131.

Amended independent claims 27 and 32 recite a chemical vapor codeposited diffusion barrier layer. In contrast to claims 27 and 32, Matsubara et al. recites a thin-film capacitor with a silicon substrate, an insulating silicon oxide layer, a lower electrode, a dielectric layer of $BaTiO_3$ and an upper electrode of aluminum layer stacked in sequence from bottom to top (Col. 3, lines 42-47). The lower electrode layer is formed by a DC magnetron sputtering technique using a target of sintered Ru or $RuSi_2$ (Col. 3, lines 53-56).

Matsubara et al. fails to teach a semiconductor device structure that includes a chemical vapor codeposited diffusion barrier layer of $RuSi_x$ over at least a portion of a surface. In other

words, Matsubara et al. describes a sputtered $RuSi_2$ electrode layer and not a chemical vapor codeposited diffusion barrier layer.

A chemical vapor deposited diffusion barrier layer according to the present invention is different than a sputtered layer such as described by Matsubara et al. For example, a sputter coated layer, particularly with respect to high aspect ratio structures, provides different coverage thereon when compared to a chemical vapor deposited layer. For example, a sputtered layer at the edge of a contact hole tends to be particularly thick, reducing the opening of the holes disproportionately or, for example, sputtered material may not reach the bottom of the contact holes.

In contrast, a chemical vapor deposited film provides a highly conformal layer within deep contacts and other openings such as for lower electrodes of storage cell capacitors. *See* Specification, page 9, lines 15-17. These highly conformal layers relative to high aspect ratio structures are generally not possible with sputter coating. Thus, the structures recited in claims 27-35, including chemical vapor codeposited layers, are physically, structurally, and patentably distinct from those recited in Matsubara et al.

The Examiner alleges that the term "chemical vapor deposited" recites "a method of forming and does not deviate from the structure of a diffusion barrier made of $RuSi_x$." As a result, the Examiner gives no patentable weight to such term. Applicants traverse this allegation.

Applicants submit that the term "chemical vapor deposited" (which has been amended to recite "chemical vapor codeposited") is not a "product by process" limitation because the term describes the structure of the barrier layer. *See Hazani v. U.S. Int'l Trade Comm.*, 44 U.S.P.Q.2d 1358, 1363 (Fed. Cir. 2000) (holding that the limitation "chemically engraved" is not a product-by-process limitation). As stated above, a chemical vapor codeposited layer is different than a sputtered layer such as described by Matsubara et al. For example, a chemical vapor codeposited layer may be more conformal than a sputtered layer, especially when considering deep contacts and other openings. Further, a CVD codeposited layer may exhibit a more uniform distribution of ruthenium and silicide throughout the layer than a layer formed by

sputtering or silicidation. Therefore, those skilled in the art would appreciate the structural differences between a chemical vapor codeposited layer and a sputtered layer. The words of a claim must be read as they would be interpreted by those of ordinary skill in the art. *See In re Sneed*, 218 U.S.P.Q. 385 (Fed. Cir. 1983). Because those skilled in the art would appreciate that a chemical vapor deposited diffusion barrier layer is structurally different than a sputtered layer, the term "chemical vapor codeposited" is to be given patentable weight in the pending claims.

Claims 28-31 and 33-35, which depend, either directly or ultimately, from either claim 27 or 32, are not anticipated by Matsubara et al. for the same reasons as presented above for claims 27 and 32. In addition, claims 28-31 and 33-35 each provide additional elements that further support patentability when combined with claims 27 and 32.

For at least the above reasons, Applicants submit that claims 27-35 are not anticipated by Matsubara et al. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

The Examiner also rejected claims 27-28, 30-33, and 36-44 under 35 U.S.C. § 102(b) as being anticipated by Kuroiwa et al. (U.S. Patent No. 6,239,460).

Applicants traverse this rejection and submit that claims 27-28, 30-33, and 36-44 are not anticipated by Kuroiwa et al. because such document does not teach each and every element of claims 27-28, 30-33, and 36-44.

For example, claims 27 and 32 each recite a chemical vapor codeposited diffusion barrier layer that is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10. In contrast to claims 27 and 32, Kuroiwa et al. teaches a capacitor that includes a metal electrode 130 deposited on the top surface of a plug 111. *See* Kuroiwa et al., column 12, lines 26-29. In the embodiment of Kuroiwa et al. relied upon by the Examiner, a ruthenium silicide layer is formed by either sputtering or chemical vapor depositing a ruthenium layer on an already formed silicon plug 111. *See* Kuroiwa et al., column 12, lines 35-36 and column 13, lines 7-18. Then a quick heat treatment is performed so that a portion of the metal electrode 130 is formed into a

ruthenium silicide layer 132. This teaching of Kuroiwa et al. is in direct contrast to that described in amended claims 27 and 32 where the $RuSi_x$ is codeposited, i.e., the $RuSi_x$ is deposited by CVD using a ruthenium precursor and a silicon precursor.

One skilled in the art would understand that a codeposited $RuSi_x$ layer exhibits many differences over a ruthenium silicide layer formed by silicidation as taught by Kuroiwa et al. For example, a CVD codeposited $RuSi_x$ layer may include a more uniform distribution of silicon throughout the layer, whereas a silicidated ruthenium silicide layer may exhibit a gradient of silicon content from the ruthenium/silicon interface to the opposite surface of the ruthenium layer. Further, a silicidated ruthenium silicide layer may include uneven island formations of silicide instead of a more uniform $RuSi_x$ formed by CVD codeposition.

Further, for example, claim 36 recites an interconnect that includes a chemical vapor deposited diffusion barrier layer. An interconnect may include, for example, conductive layers in contact holes, vias, etc. *See* Specification, page 1, lines 13-14. In contrast to claim 36, the embodiment of Kuroiwa et al. relied upon by the Examiner teaches a capacitor structure. *See*, e.g., Office Action, page 2 ("Regarding claims 32, 33 and 36-44, Kuroiwa shows (*see*, for example, FIG. 10) a capacitor structure comprising metal electrode (first electrode) 130, capacitor dielectric 115 and upper electrode (second electrode) 116."). In other words, Kuroiwa et al. does not teach an interconnect that includes a chemical vapor deposited diffusion barrier layer.

Claims 28, 30-31, 33, and 37-44 each depend, either directly or ultimately, from one of claims 27, 32, and 36. As such, claims 28, 30-31, 33, and 37-44 are not anticipated by Kuroiwa et al. for the same reasons as presented above for claims 27, 32, and 36. In addition, claims 28, 30-31, 33, and 37-44 each recite additional elements that further support patentability when combined with claims 27, 32, and 36.

For at least the above reasons, Applicants submit that claims 27-28, 30-33, and 36-44 are not anticipated by Kuroiwa et al. Reconsideration and withdrawal of this rejection are, therefore, respectfully requested.

Amendment and Response
Applicant(s): Vaartstra et al.
Serial No.: 09/603,132
Confirmation No.: 3538
Filed: 23 June 2000
For: DEVICE STRUCTURES INCLUDING RUTHENIUM SILICIDE DIFFUSION BARRIER LAYERS

Summary

It is respectfully submitted that the pending claims are in condition for allowance and notification to that effect is respectfully requested. The Examiner is invited to contact Applicants' Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

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CERTIFICATE UNDER 37 C.F.R. § 1.8:
The undersigned hereby certifies that this paper is being transmitted by facsimile in accordance with 37 C.F.R. § 1.6(d) to the Patent and Trademark Office, addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on this 18 day of September, 2002, at 1:10 p.m. (Central Time).

By: [signature]
Name: Sara E. Olson

APPENDIX A - CLAIM AMENDMENTS
INCLUDING NOTATIONS TO INDICATE CHANGES MADE
Serial No.: 09/603,132
Docket No.: 150.00650102

Amendments to the following are indicated by underlining what has been added and bracketing what has been deleted.

In the Claims

For convenience, all pending claims are shown below.

27. **(Thrice Amended)** A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a chemical vapor [deposited]codeposited diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

28. The structure of claim 27, wherein x is in the range of about 1 to about 3.

29. The structure of claim 28, wherein x is about 2.0.

30. The structure of claim 27, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

31. The structure of claim 30, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

32. **(Thrice Amended)** A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a chemical vapor [deposited]codeposited diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

33. The structure of claim 32, wherein x is in the range of about 1 to about 3.

34. The structure of claim 32, wherein the first electrode comprises a diffusion barrier layer, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region, and further wherein the first electrode comprises one or more additional conductive layers formed over the diffusion barrier layer, the one or more additional conductive layers formed of at least one of a metal and a conductive metal oxide.

35. The structure of claim 34, wherein the one or more additional conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, and Ir.

36. **(Thrice Amended)** [A]An integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a chemical vapor deposited diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

37. The structure of claim 36, wherein x is in the range of about 1 to about 3.

38. The structure of claim 36, further comprising a conductive contact material formed relative to the diffusion barrier layer.

39. The structure of claim 27, wherein the surface of the substrate assembly defines an opening, where the diffusion barrier layer is on the surface defining the opening.

40. The structure of claim 39, wherein the opening has an aspect ratio greater than about 1.

41. The capacitor structure of claim 32, wherein the capacitor structure includes a surface defining an opening, and wherein the first electrode comprises a diffusion barrier layer formed on the surface defining the opening.

42. The capacitor structure of claim 41, wherein the opening has an aspect ratio greater than about 1.

43. The capacitor structure of claim 42, wherein the opening has an aspect ratio greater than about 1.

44. The capacitor structure of claim 43, wherein the diffusion barrier layer comprises a conformal layer of uniform thickness within the opening.